

FIG. 1

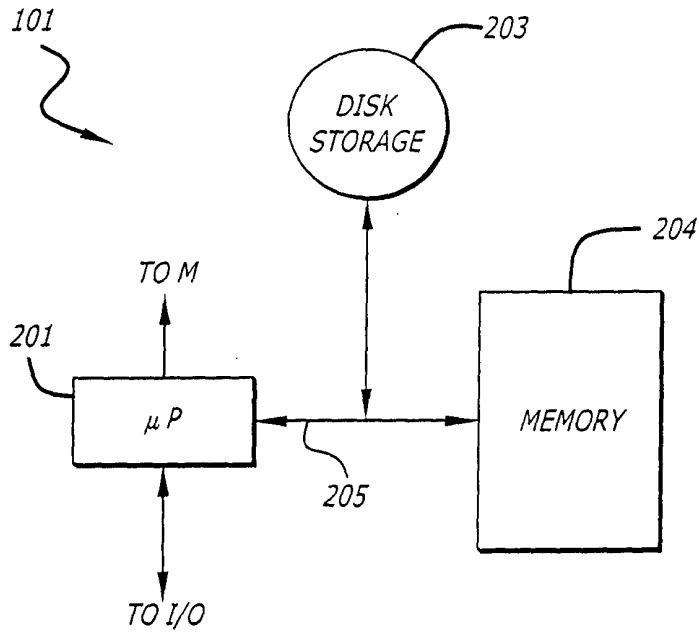
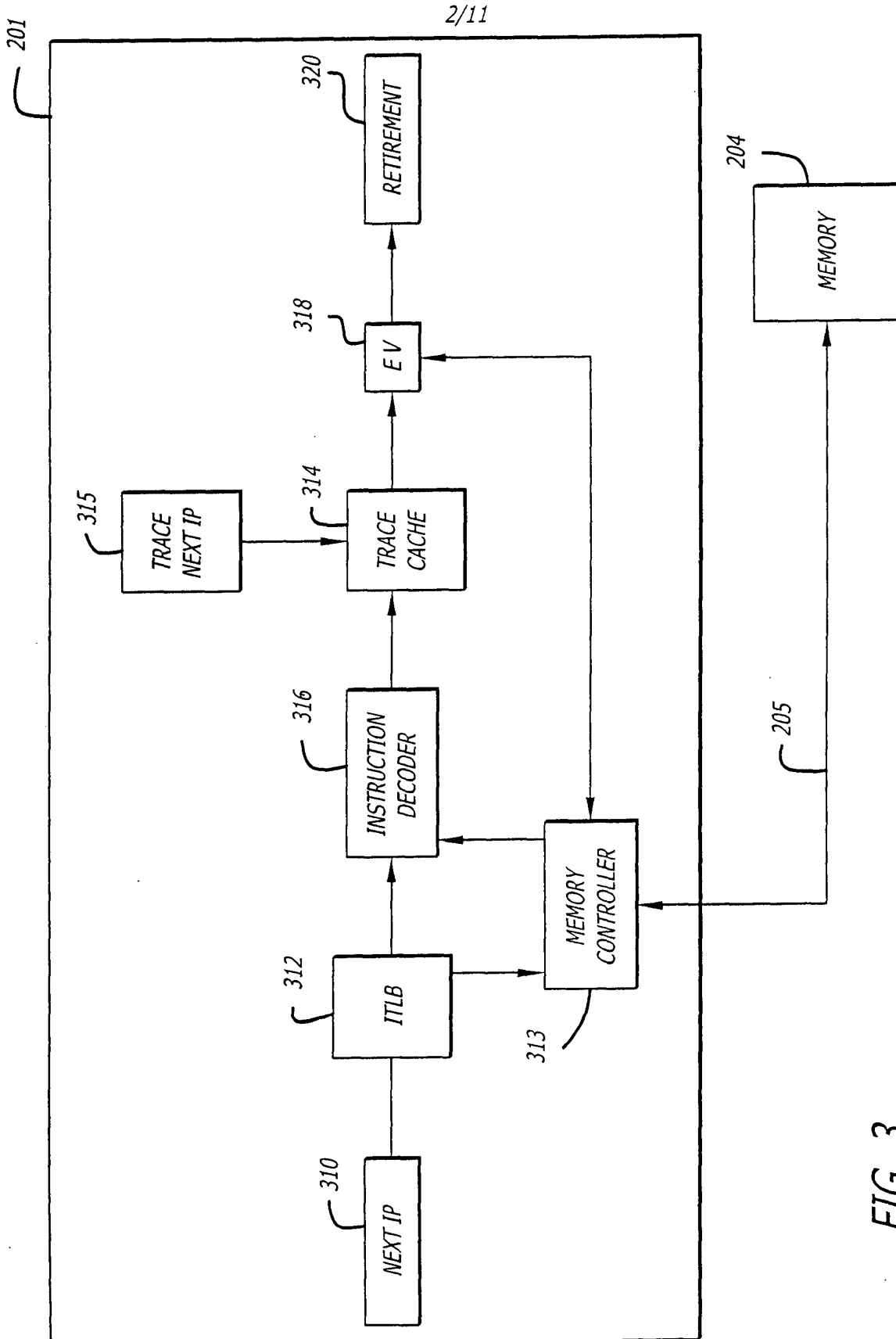


FIG. 2



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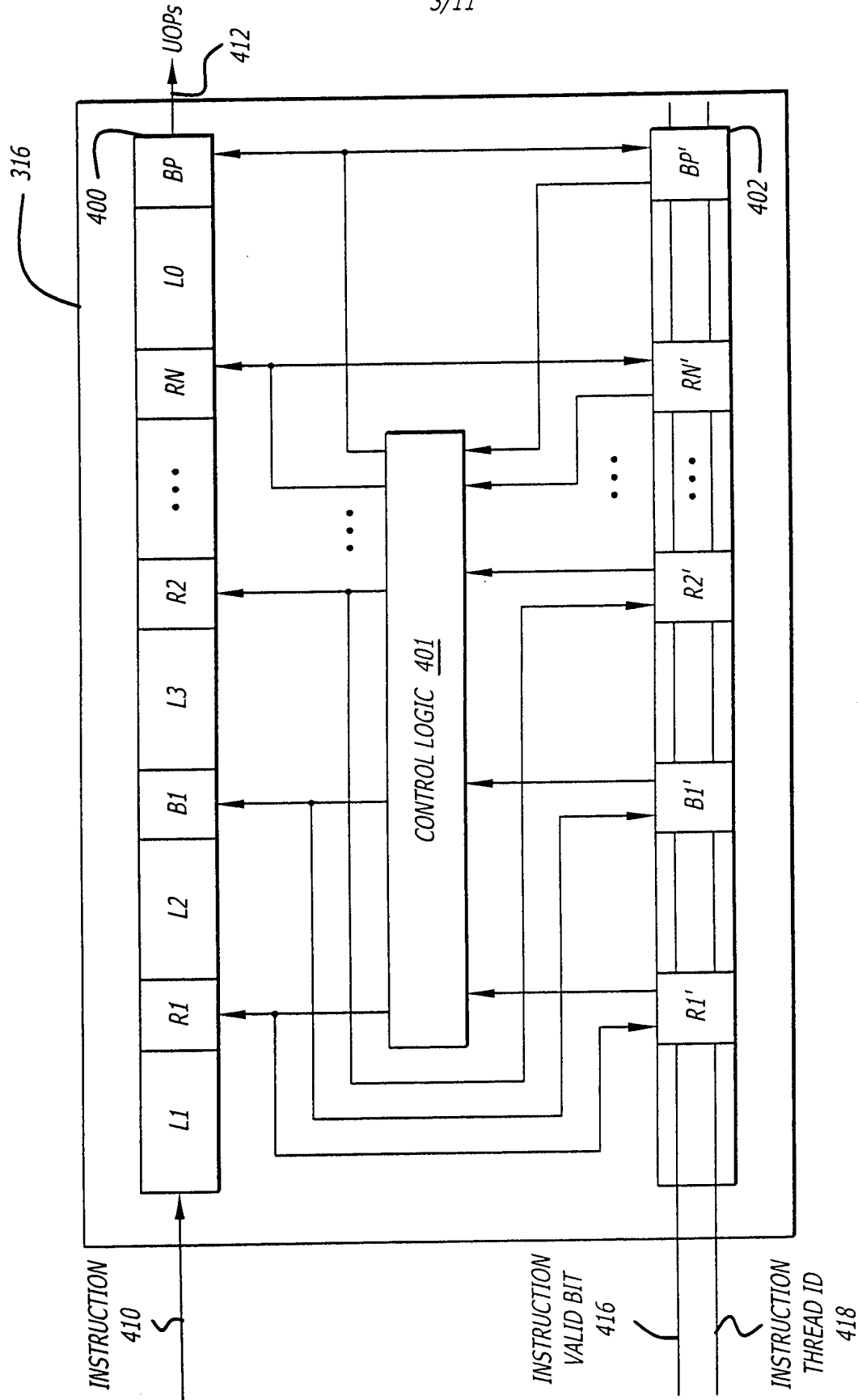


FIG. 4

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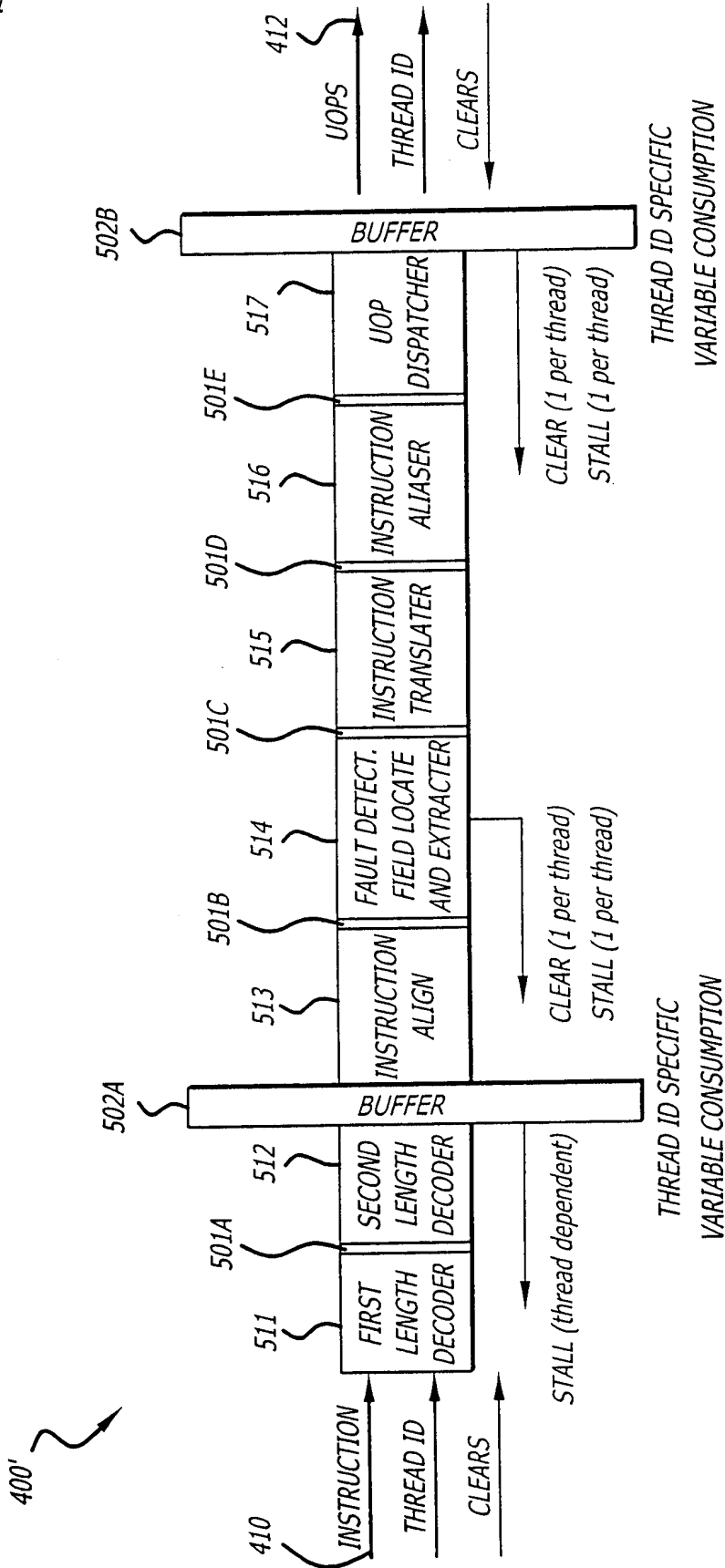
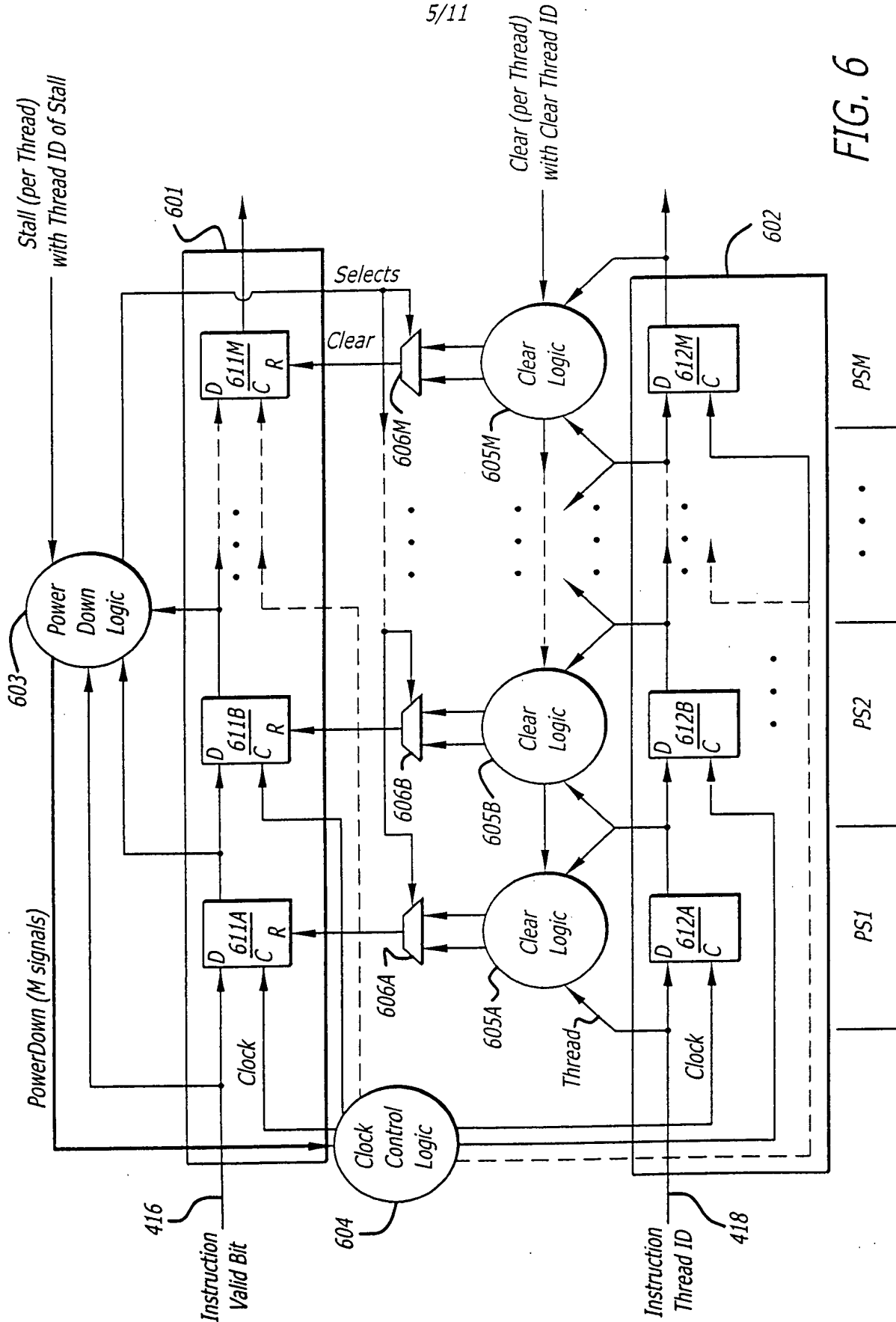


FIG. 5

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Stall for Next to Last PipeStage (NLP)

$\text{Stall}_{(NLP)} = \text{Valid Instruction in Pipe}_{(NLP)} \text{ AND } (\text{ThreadId}_{(NLP)} = \text{ThreadId of Stall})$

Stall for any other PipeStage X

$\text{Stall}_{(X)} = \text{Valid Instruction in Pipe}_{(X)} \text{ AND Valid Instruction in Pipe}_{(X+1)} \text{ AND Stall}_{(NLP)}$

Powerdown for any PipeStage X

$\text{Powerdown}_{(X)} = \text{NOT Valid Instruction in Pipe}_{(X-1)}$

Clock Enable for any PipeStage X

$\text{Clock}_{(X)} = \text{NOT Stall}_{(X)} \text{ AND NOT Powerdown}_{(X)}$

Clock for any PipeStage X

$\text{Clear}_{(X)} = \text{Clock}_{(X)} \text{ AND } [(\text{ClearThread}_{(Id0)} \text{ AND } (\text{ThreadId}_{(X-1)} = Id0)) \text{ OR } (\text{ClearThread}_{(Id1)} \text{ AND } (\text{ThreadId}_{(X-1)} = Id1))]$

OR

$\text{NOT Clock}_{(X)} \text{ AND } [(\text{ClearThread}_{(Id0)} \text{ AND } (\text{ThreadId}_{(X)} = Id0)) \text{ OR } (\text{ClearThread}_{(Id1)} \text{ AND } (\text{ThreadId}_{(X)} = Id1))]$

$\text{ClearThread}_{(Id0)} = \text{There was a Clear on Thread Identification 0}$

$\text{ClearThread}_{(Id1)} = \text{There was a Clear on Thread Identification 1}$

$\text{Pipe}_{(X)} = \text{Any pipestage in the decode}$

$\text{Pipe}_{(X-1)} = \text{Pipestage before Pipe}_{(X)}$

$\text{Pipe}_{(X+1)} = \text{Pipestage after Pipe}_{(X)}$

FIG. 7

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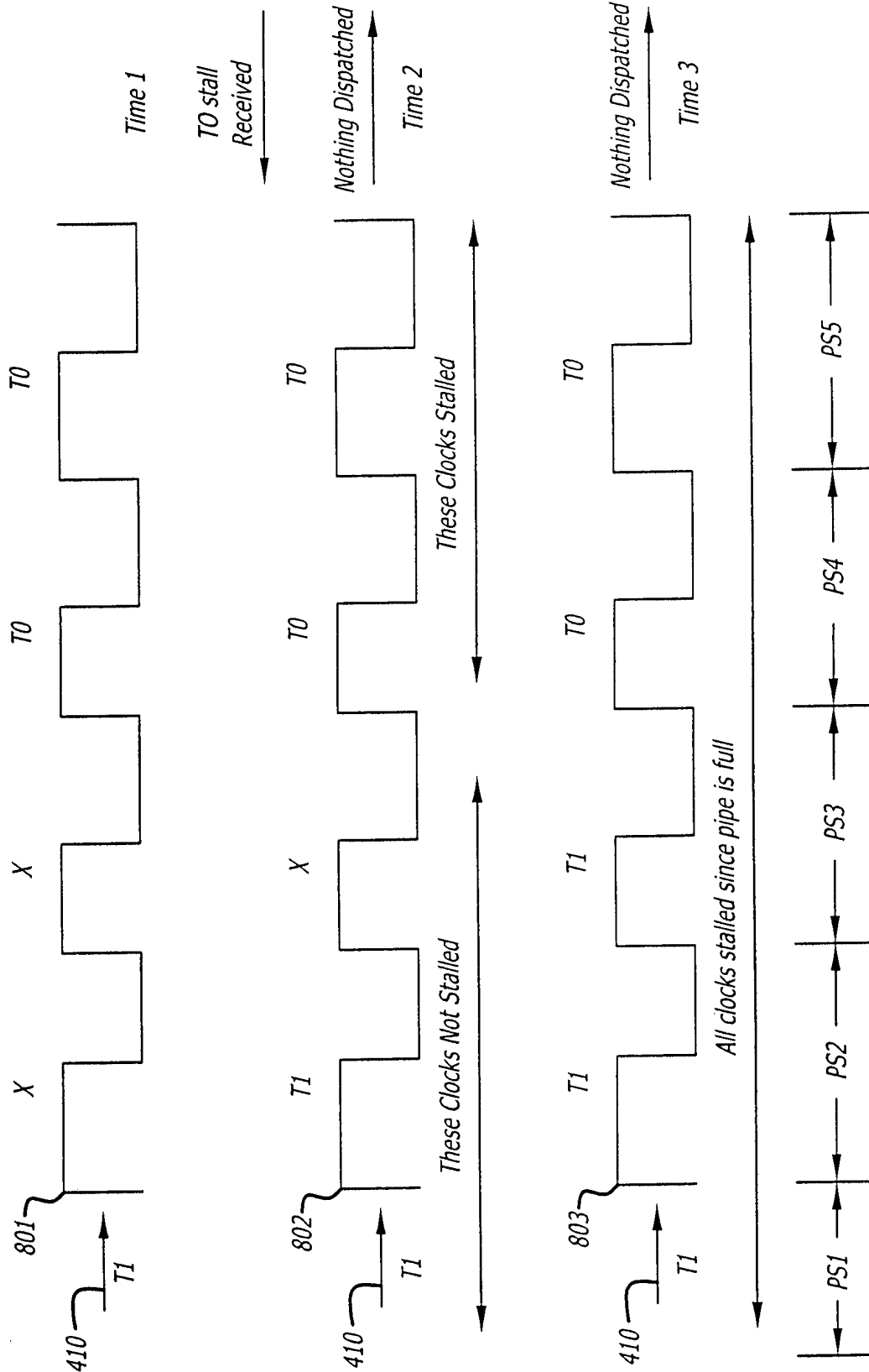


FIG. 8

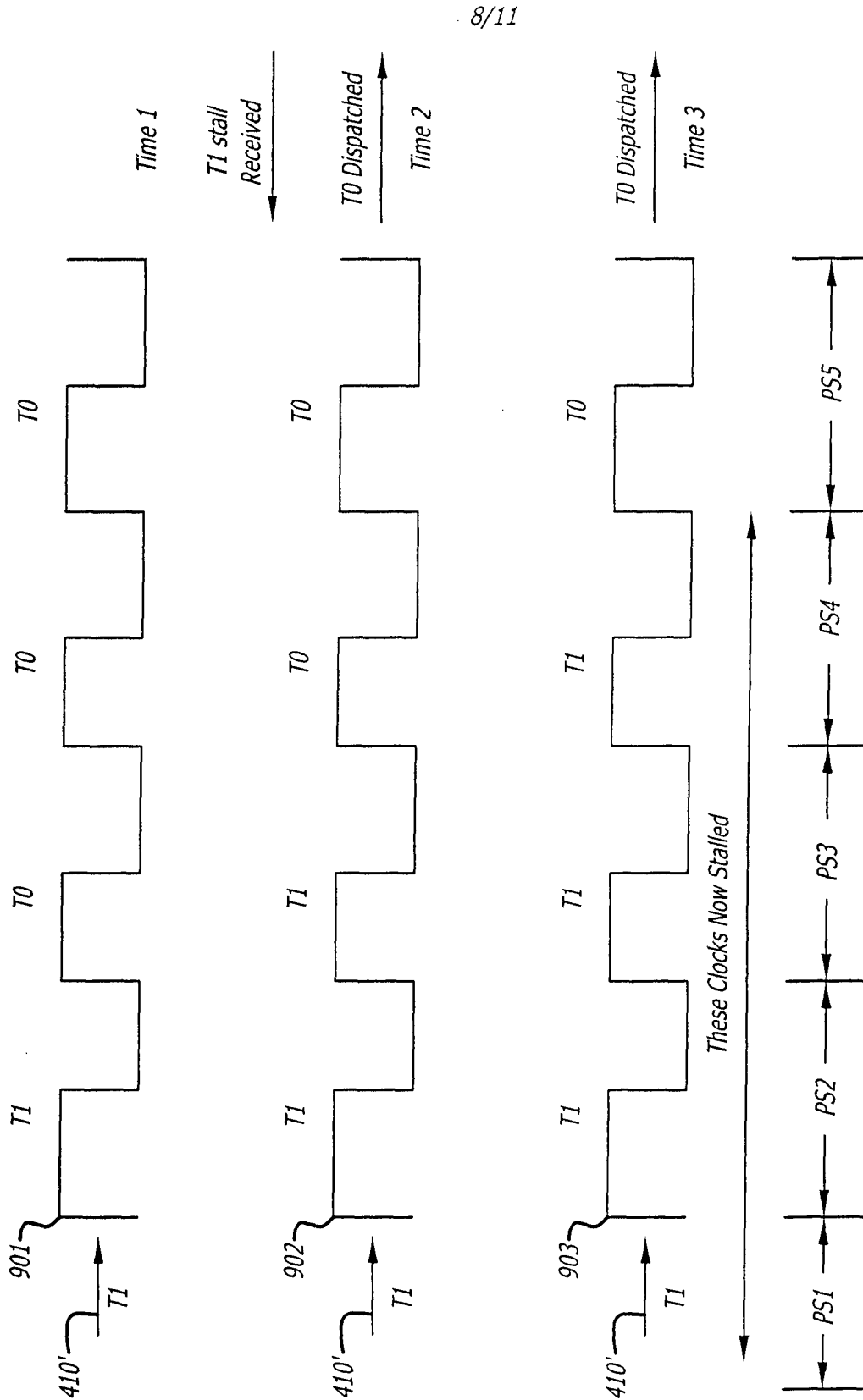


FIG. 9

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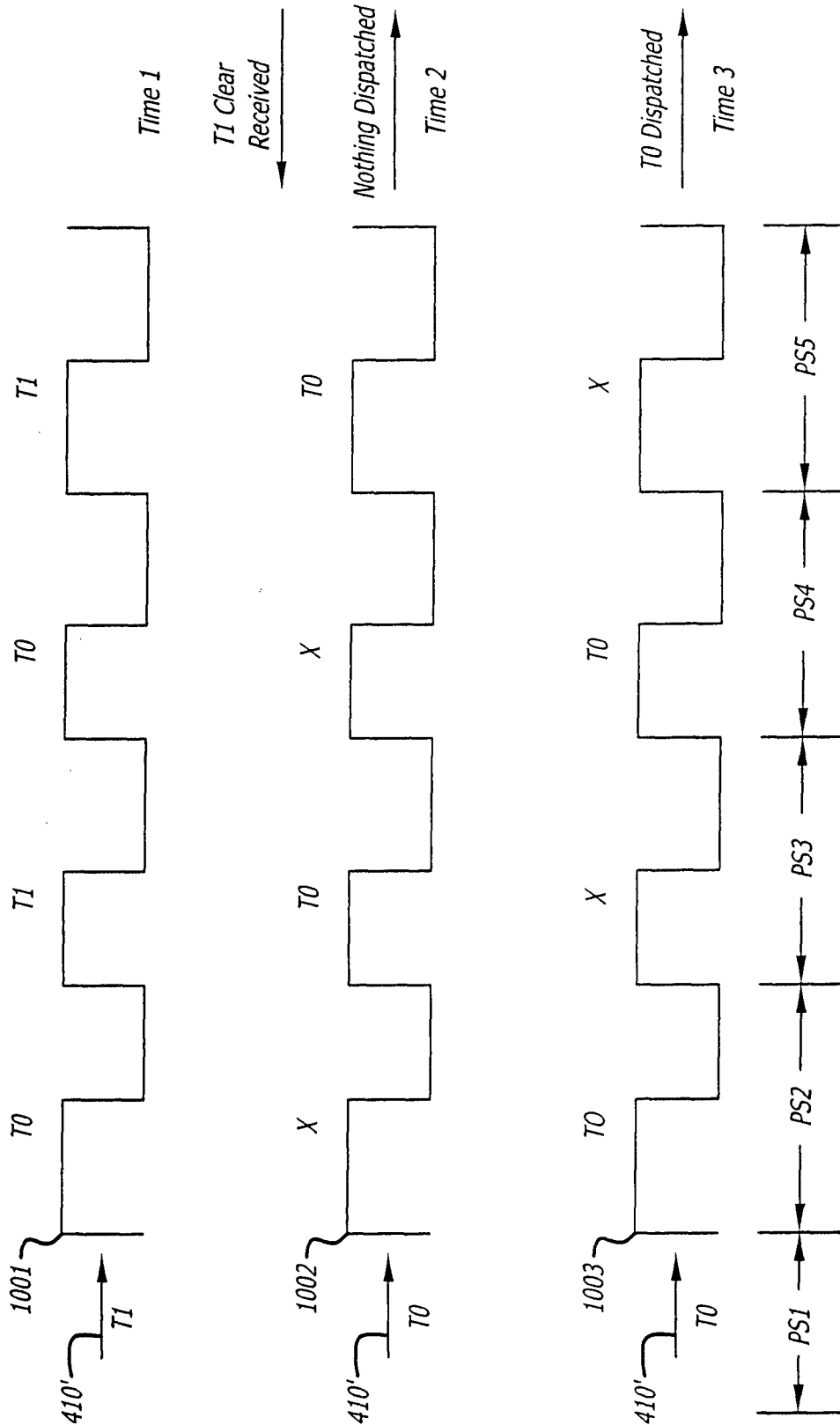


FIG. 10

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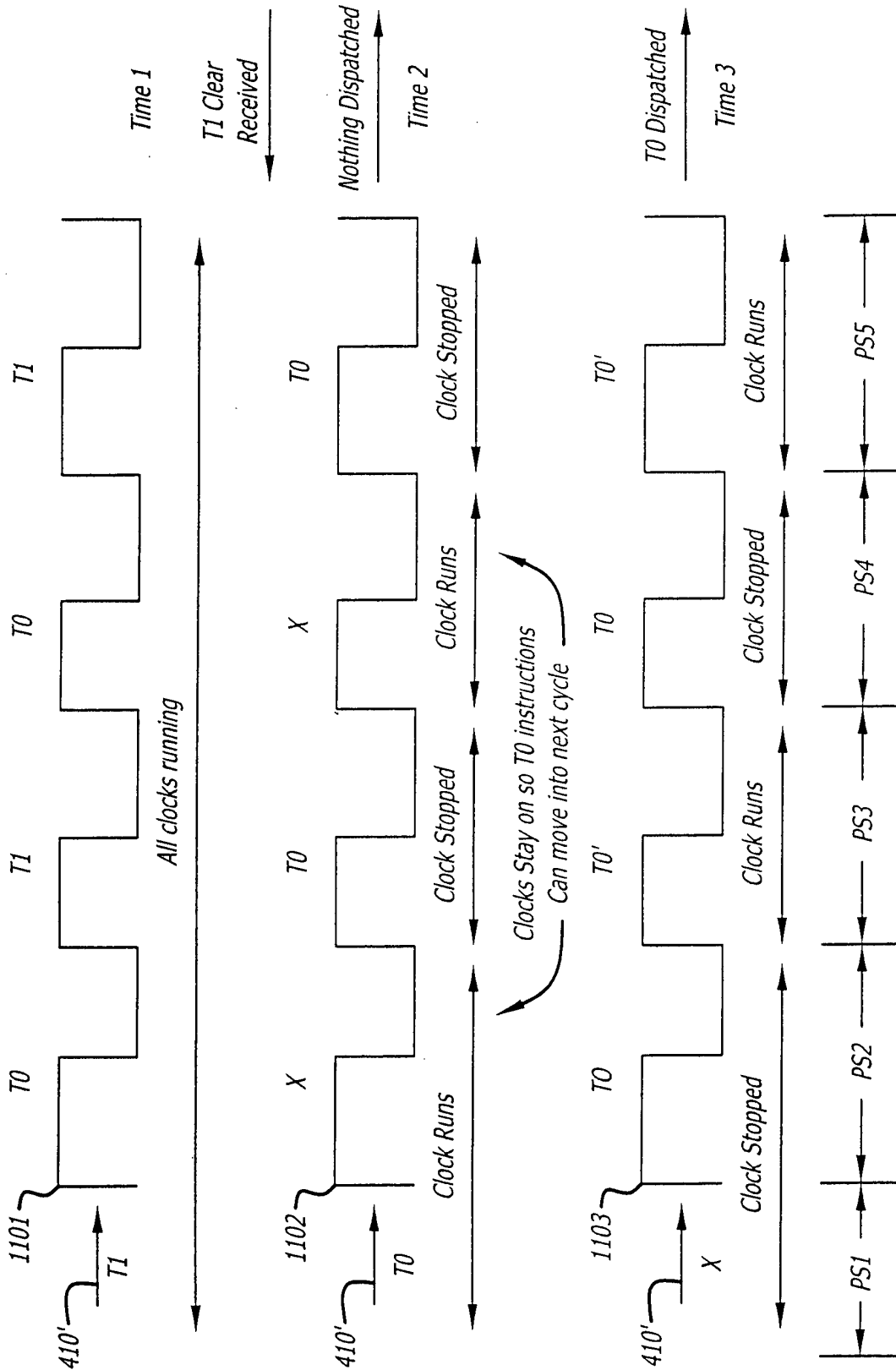


FIG. 11A

